ČESKÉ VYSOKÉ UČENÍ TECHNICKÉ V PRAZE
Fakulta elektrotechnická

CZECH TECHNICAL UNIVERSITY IN PRAGUE
Faculty of Electrical Engineering

Analysis of Nonlinear Radio Frequency and Microwave Circuits

Analýza nelineárních vysokofrekvenčních a mikrovlnných obvodů

Ing. Josef Dobeš, CSc.

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Summary

The lecture deals with the analysis of nonlinear radio frequency and microwave circuits using computer-aided design (CAD) from the point of view model and algorithm aspects.

In the first part of the presentation, two ways for improving the accuracy and robustness of the standard models of GaAsFET and MOSFET are introduced. For the GaAsFET model, a simple but important improvement of the equations for the primary voltage-controlled current source is defined. The updated model is able to represent not only GaAsFETs, but also pHEMTs in a precise way. For the MOSFET model, smoothing the discontinuities of the two dimensional gate capacitance functions is also defined. The suggested exponential smoothing leads to the reliable analyses of large digital and analog CMOS integrated circuits using CAD.

The second part of the presentation deals with the algorithm for solving the nonlinear systems of algebraic-differential equations. The algorithm is able to solve stiff systems too, generates accurate results regardless the model type, and has an interface to other methods for analyzing the RF and microwave systems as steady-state or time domain sensitivity algorithms. The incorporation of the time domain sensitivity analysis is accomplished using a new effective recurrent formula. In the habilitation thesis, a special attention is dedicated to the ways for automatic determining the integration step lengths and the order of interpolation polynomials, and to protecting the convergence.

Finally, two practical examples are solved from the area of the radio frequency integrated circuits design. The first one has come from the digital circuits domain—a fragment of a large integrated circuit containing CMOS RF flip-flops is analyzed as a sophisticated test of the modified model and algorithm. The second one has come from the analog circuits domain—a low-voltage low-power CMOS RF multiplier is analyzed as a convenient test of the new recurrent formula in the time domain sensitivity analysis.

Souhrn

Přednáška je zaměřena na analýzu nelineárních vysokofrekvenčních a mikrovlnných obvodů počítačem z hlediska zdokonalování modelů a algoritmů.

Úvodní část prezentace je věnována metodám zlepšování přesnosti a robustnosti standardních modelů GaAsFET a MOSFET. V modelu GaAsFET je navrženo jednoduché, ale důležité zdokonalení rovnic základního napěťově řízeného proudového zdroje modelu. Modifikované vztahy zpřesňují model GaAsFET, jsou však vhodné i k charakterizování pHEMT. V modelu MOSFET je navrženo vyhlazování nespojitostí dvojdimenzionální funkce hradlové kapacity. Použitý způsob exponenciálního vyhlazování zajišťuje spolehlivost analýz rozsáhlých číslicových a analogových integrovaných obvodů v technologii CMOS nástroji CAD.

Druhá část prezentace je věnována algoritmu pro řešení nelineárních soustav algebraicko-diferenciálních rovnic. Algoritmus musí být schopen řešit systémy charakterizované řádově odlišnými časovými konstantami, poskytuje přesné výsledky bez ohledu na použitou formu modelu a má rozhraní k dalším metodám pro analýzu vysokofrekvenčních a mikrovlnných systémů jako ustalovací algoritmus nebo algoritmus citlivostní analýzy v časové oblasti. Začlenění citlivostní analýzy v časové oblasti je provedeno implementací nového efektivního rekurentního vztahu. V habilitační práci se věnuje velká pozornost automatickému určování délky integračního kroku i řádu interpolačního polynomu a zajištění spolehlivé konvergence.

Závěrem je předvedeno řešení dvou praktických příkladů z oblasti návrhu vysokofrekvenčních integrovaných obvodů. První příklad je z oblasti číslicových integrovaných obvodů – jde o fragment rozsáhlého systému obsahujícího vysokofrekvenční klopné obvody CMOS, který slouží jako náročný test modifikovaného modelu a algoritmu. Druhý příklad je z oblasti analogových integrovaných obvodů – jde o nízkonapěťovou vysokofrekvenční násobičku CMOS, která slouží jako vhodný test nového rekurentního vztahu citlivostní analýzy v časové oblasti.

Keywords:

GaAsFET, MOSFET, device characterization, circuit modeling, numerical integration, predictor, corrector, logarithmic damping, sensitivity analysis, CMOS technology, flip-flop, radio frequency circuits, microwave circuits, four-quadrant multiplier, mixer

Klíčová slova:

GaAsFET, MOSFET, charakterizování prvků, modelování obvodů, numerická integrace, prediktor, korektor, logaritmické tlumení, citlivostní analýza, technologie CMOS, klopný obvod, vysokofrekvenční obvody, mikrovlnné obvody, čtyřkvadrantová násobička, směšovač

Contents

1 Preface

The area of analyzing the nonlinear RF and microwave circuits using CAD naturally consists of two parts. First, a set of accurate and numerically stable models must be established, especially the models of RF and microwave semiconductor devices and transmission lines. Second, a robust and efficient algorithm for solving the nonlinear systems of algebraic-differential equations must be developed. The algorithm must be able to solve stiff systems too and must have an interface to other methods for analyzing the RF and microwave systems as steady-state or time domain sensitivity algorithms. In the lecture, some uncomplicated, but efficient improvements of the GaAsFET and MOSFET models are presented. Furthermore, main features of the stable algorithm for solving the nonlinear algebraic-differential equations are summarized including the time domain sensitivity analysis. Two practical examples are solved to prove the model and algorithm properties.

2 Refinement of the Semiconductor Device Models

Two improvements of the GaAsFET and MOSFET models are presented in this section. As an example in the static domain, updating the standard GaAsFET current function is defined with the effect to the precision of the model. As an example in the time domain, smoothing the standard MOSFET gate capacitance function is proposed with the effect to the robustness of the model. The new models are built into the author's program C.I.A.

2.1 Improving the Accuracy of the GaAsFET Model

2.1.1 Updating the Model Equations

The primary voltage-controlled current source of the GaAsFET model can be defined for the forward mode ($V_{\mathrm{DS}} \geqq 0$) by the updated equations [6]

$$V_{T1} = V_{T0}\boxed{-\sigma V_{\mathrm{DS}}}, \tag{1a}$$

$$I_{\mathrm{D}} = \begin{cases} 0 & \text{for } V_{\mathrm{GS}} \leqq V_{T1}, \\ \beta\,(V_{\mathrm{GS}} - V_{T1})^{n_2}\,(1 + \lambda V_{\mathrm{DS}})\tanh(\alpha V_{\mathrm{DS}}) & \text{otherwise,} \end{cases} \tag{1b}$$

and for the reverse mode ($V_{\mathrm{DS}} < 0$) by the mirrored equations

$$V_{T1} = V_{T0}\boxed{+\sigma V_{\mathrm{DS}}}, \tag{2a}$$

$$I_{\mathrm{D}} = \begin{cases} 0 & \text{for } V_{\mathrm{GD}} \leqq V_{T1}, \\ \beta\,(V_{\mathrm{GD}} - V_{T1})^{n_2}\,(1 - \lambda V_{\mathrm{DS}})\tanh(\alpha V_{\mathrm{DS}}) & \text{otherwise.} \end{cases} \tag{2b}$$

The model parameters V_{T0}, β, n_2, λ and α have already been defined in [14], the parameter σ used in the "boxed" parts of (1) and (2) represents an improvement of the classical simpler models—it creates a "modified" threshold voltage V_{T1}. The Parker-Skellern realistic model [9] contains similar functions—(1a) and (2a) can be considered their base.

Although the equations (1) and (2) are relatively very simple, they contain an important improvement in comparison with the classical Curtice model [1] (n_2 which characterizes *gate-source* voltage influence more precisely), and also in comparison with the classical Statz model [13] (σ which characterizes *drain-source* voltage influence more precisely).

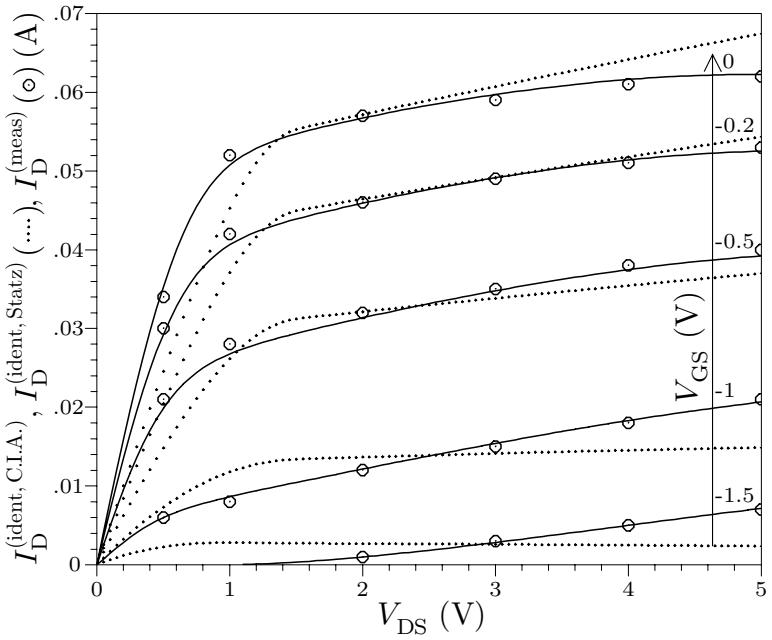

Figure 1: Comparison of the GaAsFET model identification using the suggested and classical Statz equations (the root mean square error is only 2.73 % for the C.I.A. model). The measured data including r_D and r_S estimations are taken from [7].

2.1.2 Identifying the Model Parameters

The importance of the modifications (1a) and (2a) can be demonstrated by the identification of the model parameters for DZ71 [7] GaAsFET—see the results in Figure 1. The C.I.A. optimization procedure [2] has provided the values of the model parameters $V_{T0} = -1.36\,\mathrm{V}$, $\beta = 0.0346\,\mathrm{A\,V^{-2}}$, $n_2 = 1.73$, $\lambda = -0.082\,\mathrm{V^{-1}}$ (negative value arises if σ used), $\alpha = 2.56$, $\sigma = 0.141$, $r_D = 2.88\,\Omega$, and $r_S = 2.62\,\Omega$ (r_D and r_S have already been estimated in [7]). To compare, the same FET has been identified by the classical Statz model [13]—the proposed model is more accurate, especially for the lesser values of V_{GS}.

2.1.3 Using the Updated GaAsFET Model as the pHEMT Representation

The modifications (1a) and (2a) also enable the model to be used for the pHEMT modeling [6]. For such devices, the model is also able to form a *negative* differential conductance obtained using a static measurement. On the other hand, at very high frequencies, the s_{22} parameter has mostly a *positive* real part. Therefore, a corrective current source [6] must be added identified by the s parameters measurement. Embedding the frequency dispersion can also be performed in another precise, but more complicated way—see [9].

2.2 Improving the Robustness of the MOSFET Model

The gate capacitance models have been thoroughly defined for the gate-source controlling voltage. However, the models need a refinement for the case of a large drain-source voltage variation, especially if the drain-source voltage changes its sign. Therefore, an idea of the exponential smoothing of the model discontinuities has been suggested [5]. The method is able to suppress non-convergences which occur due to the drain-source sign alternations.

2.2.1 Necessity for Ensuring the Convergence

The SPICE3 program uses the Meyer's voltage controlled model, the programs of the PSPICE family [15] contain both the same model and the Ward's charge controlled model at several levels, especially for the BSIM class. In most cases, the models do not have problems related to gate-source voltage changes. However, if the drain-source voltage changes its sign during a transient analysis, the problems with convergence can occur. Such problems are described in [8, pp. 197–198] for both Meyer's and Ward's models. For that reason, a requirement for an updated model can be defined as

$$\lim_{V_{\mathrm{DS}}\to 0+} C_{\mathrm{GS}} = \lim_{V_{\mathrm{DS}}\to 0-} C_{\mathrm{GS}} \wedge \lim_{V_{\mathrm{DS}}\to 0+} C_{\mathrm{GD}} = \lim_{V_{\mathrm{DS}}\to 0-} C_{\mathrm{GD}} \tag{3}$$

for the Meyer's model and (see the definition of related charges in [8, pp. 210–211])

$$\lim_{V_{\mathrm{DS}}\to 0+} \dot{Q}_S = \lim_{V_{\mathrm{DS}}\to 0-} \dot{Q}_S \wedge \lim_{V_{\mathrm{DS}}\to 0+} \dot{Q}_D = \lim_{V_{\mathrm{DS}}\to 0-} \dot{Q}_D \tag{4}$$

for the Ward's model.

2.2.2 Discontinuities of the Classical Models

The problem with discontinuities can easily be demonstrated on the classical Meyer's model, which is defined in [15] in a simple form and in [8] in a complete form. However, the actual implementation in the new SPICE programs slightly differs from that in [8]. Therefore, let's define the updated model in the complete form with all the discontinuities to be considered. The definition of the Meyer's gate capacitance model splits for the normal mode ($V_{\mathrm{DS}} \geqq 0$) into the following regions:

- accumulation region—for $V_{\mathrm{GS}} - V_{\mathrm{on}} \leqq -\phi_S$:

$$\begin{aligned} C_{\mathrm{GB}} &= C_{\mathrm{ox}}, \\ C_{\mathrm{GS}} &= 0, \\ C_{\mathrm{GD}} &= 0, \end{aligned} \tag{5a}$$

- transition region—for $-\phi_S < V_{\mathrm{GS}} - V_{\mathrm{on}} \leqq -\dfrac{\phi_S}{2}$:

$$\begin{aligned} C_{\mathrm{GB}} &= -C_{\mathrm{ox}} \frac{V_{\mathrm{GS}} - V_{\mathrm{on}}}{\phi_S}, \\ C_{\mathrm{GS}} &= 0, \\ C_{\mathrm{GD}} &= 0, \end{aligned} \tag{5b}$$

- depletion region—for $-\dfrac{\phi_S}{2} < V_{\mathrm{GS}} - V_{\mathrm{on}} \leqq 0$:

$$\begin{aligned} C_{\mathrm{GB}} &= -C_{\mathrm{ox}} \frac{V_{\mathrm{GS}} - V_{\mathrm{on}}}{\phi_S}, \\ C_{\mathrm{GS}} &= \frac{2}{3} C_{\mathrm{ox}} \left(2 \frac{V_{\mathrm{GS}} - V_{\mathrm{on}}}{\phi_S} + 1 \right), \\ C_{\mathrm{GD}} &= 0, \end{aligned} \tag{5c}$$

- saturation region—for $0 < V_{\rm GS} - V_{\rm on} \leqq V_{\rm DS}$:

$$\begin{aligned} C_{\rm GB} &= 0, \\ C_{\rm GS} &= \frac{2}{3} C_{\rm ox}, \\ C_{\rm GD} &= 0, \end{aligned} \tag{5d}$$

- linear region—for $V_{\rm GS} - V_{\rm on} > V_{\rm DS}$:

$$\begin{aligned} C_{\rm GB} &= 0, \\ C_{\rm GS} &= \frac{2}{3} C_{\rm ox} \left\{ 1 - \left[\frac{V_{\rm GS} - V_{\rm on} - V_{\rm DS}}{2(V_{\rm GS} - V_{\rm on}) - V_{\rm DS}} \right]^2 \right\}, \\ C_{\rm GD} &= \frac{2}{3} C_{\rm ox} \left\{ 1 - \left[\frac{V_{\rm GS} - V_{\rm on}}{2(V_{\rm GS} - V_{\rm on}) - V_{\rm DS}} \right]^2 \right\}; \end{aligned} \tag{5e}$$

$V_{\rm on}$ voltage is defined in the static part of the model [8] and acts as a boundary between the regions of the weak and strong inversions [12], ϕ_S is the surface inversion potential, and $C_{\rm ox}$ is determined by the oxide permittivity and thickness, effective channel length and width by the classical formula (the entire updated model is shown in Figure 2)

$$C_{\rm ox} = C'_{\rm ox} L_{\rm eff} W_{\rm eff} = \frac{\epsilon_{\rm ox}}{t_{\rm ox}} L_{\rm eff} W_{\rm eff}. \tag{6}$$

Easily observed that the Meyer's modified model defined by (5) is continuous with respect to the gate-source voltage. However, if the drain-source voltage is changing its sign, whereas the gate-source voltage remains unchanged, then a discontinuity might arise. For example, suppose the gate-source voltage fulfills the condition for the saturation region, i.e., $0 < V_{\rm GS} - V_{\rm on} \leqq V_{\rm DS}$—the discontinuities arise for both source and drain capacitances

$$\lim_{V_{\rm DS} \to 0+} C_{\rm GS} = \lim_{V_{\rm DS} \to 0-} C_{\rm GD} = \frac{2}{3} C_{\rm ox}, \tag{7a}$$

$$\lim_{V_{\rm DS} \to 0-} C_{\rm GS} = \lim_{V_{\rm DS} \to 0+} C_{\rm GD} = 0 \tag{7b}$$

because in the reverse mode ($V_{\rm DS} < 0$), the roles of $C_{\rm GS}$ and $C_{\rm GD}$ *must* change. (Similarly, $V_{\rm GD}$ is the control voltage of the gate capacitance model instead of $V_{\rm GS}$ in the reverse mode.) In other words, it is natural to expect $\lim_{V_{\rm DS} \to 0} C_{\rm GS} = \lim_{V_{\rm DS} \to 0} C_{\rm GD}$, but this condition is *not* fulfilled, in general.

2.2.3 Solution of the Problem by Exponential Smoothing

The problem of discontinuity (7) can be overcome by means of the exponential factor

$$F_G = \exp\left(-\frac{V_{\rm DS}}{n_{\rm smooth} V_T} \right) \text{ for } V_{\rm DS} \geqq 0 \text{ (normal mode)}, \tag{8a}$$

$$F_G = \exp\left(+\frac{V_{\rm DS}}{n_{\rm smooth} V_T} \right) \text{ for } V_{\rm DS} < 0 \text{ (reverse mode)}, \tag{8b}$$

where $n_{\rm smooth}$ is a new model parameter [4] with a unit default value, and $V_T = kT/q$.

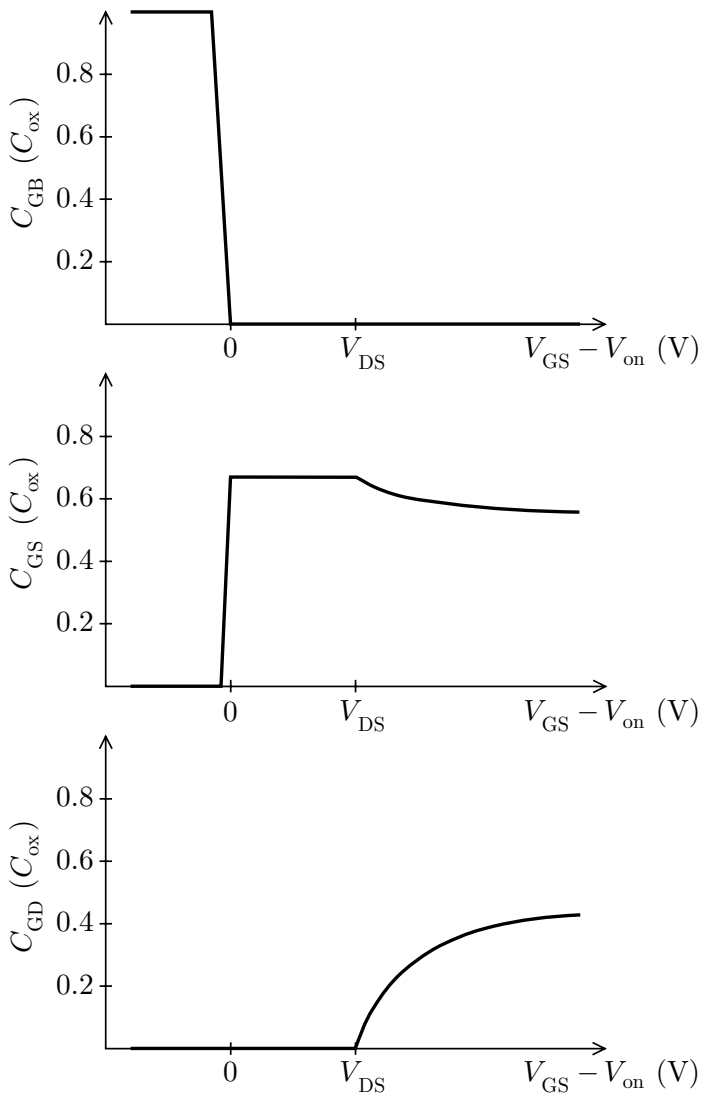

Figure 2: Updated Meyer's gate capacitance model.

For all C_{GS} and C_{GD} capacitances (5a–5e), the new ones are defined by formulae

$$C'_{\mathrm{GS}} = F_G \frac{C_{\mathrm{GS}} + C_{\mathrm{GD}}}{2} + (1 - F_G)\, C_{\mathrm{GS}}, \tag{9a}$$

$$C'_{\mathrm{GD}} = F_G \frac{C_{\mathrm{GS}} + C_{\mathrm{GD}}}{2} + (1 - F_G)\, C_{\mathrm{GD}}; \tag{9b}$$

C_{GB} capacitance does not have the problem of the discontinuity, and therefore it is left without any changes, i.e., $C'_{\mathrm{GB}} = C_{\mathrm{GB}}$. In other words, C'_{GS} and C'_{GD} capacitances are equal for $V_{\mathrm{DS}} \to 0$ now (in accordance with the physical reality—the drain and source nodes can be considered connected, when the drain-source voltage approaches zero), and they have the original unmodified values for $|V_{\mathrm{DS}}| \gg V_T$.

For the Ward's model, the problem of discontinuities related to the drain-source voltage is the same as that in the Meyer's model; moreover, the capacitances are also discontinuous related to the gate-source voltage [5]. Therefore, the problems with convergence caused by the Ward's model are expected to be considerable, and practical examples often confirm it [8]. Solving the problem of the discontinuities in the Ward's model is more difficult than that in the Meyer's one—see a more detailed procedure suggested in [5].

3 Advanced Algorithm for Solving the Nonlinear Systems of Algebraic-Differential Equations

There is a very detailed derivation in [8, pp. 197–202] proving that the typical SPICE integration algorithm (e.g., a trapezoidal scheme demonstrated in [8]) in conjunction with the Meyer's model defined in Section 2 may cause *physically incorrect* results for the circuits with isolated nodes. For this and many other reasons including a possibility to compute dynamic sensitivities, a special, robust, and very flexible algorithm has been developed. The algorithm has also been built into the author's program C.I.A., which has been used for solving sophisticated test examples presented in the following section.

3.1 Fundamental Formulae of the Implicit Integration Method

The system of algebraic-differential equations of a circuit is generally defined in an implicit form

$$\boldsymbol{f}\,[\,\boldsymbol{x}(t), \dot{\boldsymbol{x}}(t), t\,] = \boldsymbol{0}. \tag{10}$$

Let's assume now that the first n steps of a numerical integration of (10) have finished. To make equations simpler, let's mark $\boldsymbol{x}(t_n)$ by $\boldsymbol{x}_n$, and define backward scaled differences by the recurrent formulae

$$\begin{aligned} &\delta^{(0)}\boldsymbol{x}_n = \boldsymbol{x}_n, \\ &\delta^{(i)}\boldsymbol{x}_n = \delta^{(i-1)}\boldsymbol{x}_n - \alpha_n^{(i-1)}\delta^{(i-1)}\boldsymbol{x}_{n-1},\ i = 1, \ldots, k_n + 2, \end{aligned} \tag{11}$$

where k_n is the order of a polynomial interpolation used in the last integration step and

$$\begin{aligned} &\alpha_n^{(0)} = 1, \\ &\alpha_n^{(i)} = \alpha_n^{(i-1)} \frac{t_n - t_{n-i}}{t_{n-1} - t_{n-1-i}},\ i = 1, \ldots, k_n + 1. \end{aligned} \tag{12}$$

3.1.1 The Predictor

The prediction of the values for the next chosen time (i.e., for t_{n+1}) marked by $\boldsymbol{x}_{n+1}^{(0)}$ is determined by the extrapolation using the backward scaled differences (11) in the *explicit* form (it is a more sophisticated form of the Newton interpolation polynomial—see [5])

$$\boldsymbol{x}_{n+1}^{(0)} = \sum_{i=0}^{k_{n+1}} \alpha_{n+1}^{(i)} \delta^{(i)} \boldsymbol{x}_n. \tag{13}$$

Differentiating (13) with respect to t_{n+1}, the predictor of derivatives may be expressed as

$$\dot{\boldsymbol{x}}_{n+1}^{(0)} = \sum_{i=0}^{k_{n+1}} \beta_{n+1}^{(i)} \delta^{(i)} \boldsymbol{x}_n, \tag{14}$$

where the β multipliers may simply be derived from the recurrent form (12) in terms of the α ones (using (15) in (14) needs replacing the subscript n by $n + 1$, of course)

$$\begin{aligned} &\beta_n^{(0)} = 0, \\ &\beta_n^{(i)} = \frac{\alpha_n^{(i-1)} + (t_n - t_{n-i})\beta_n^{(i-1)}}{t_{n-1} - t_{n-1-i}},\ i = 1, \ldots, k_n. \end{aligned} \tag{15}$$

3.1.2 The Corrector

The correction of the values $\boldsymbol{x}_{n+1}^{(j_{\max})} \to \boldsymbol{x}_{n+1}$ for t_{n+1} is determined by using the modified Newton iterations (the symbol x marks an element of the vector $\boldsymbol{x}$)

$$\left[\left(\frac{\partial \boldsymbol{f}}{\partial \boldsymbol{x}}\right)_{n+1}^{(j)} + \left(\frac{\partial \boldsymbol{f}}{\partial \dot{\boldsymbol{x}}}\right)_{n+1}^{(j)} \underbrace{\left(\frac{\mathrm{d}\dot{x}}{\mathrm{d}x}\right)_{n+1}}_{\gamma_{n+1}}\right] \Delta \boldsymbol{x}_{n+1}^{(j)} = -\boldsymbol{f}_{n+1}^{(j)},\ j = 0, \ldots, j_{\max} < \texttt{MAXIT} \tag{16}$$

(the parameter `MAXIT` is a maximum number of iterations in one integration step), i.e., by repeated solving the linear system (16) with applying the *implicit* form of the derivatives approximation (the proof of that formula doing "algebraization" is also performed in [5])

$$\dot{\boldsymbol{x}}_{n+1}^{(j)} = \lim_{t_{n+2} \to t_{n+1}} \frac{\boldsymbol{x}_{n+2}^{(j)} - \boldsymbol{x}_{n+1}}{t_{n+2} - t_{n+1}} = \sum_{i=1}^{k_{n+1}} \frac{1}{t_{n+1} - t_{n+1-i}}\, \delta^{(i)} \boldsymbol{x}_{n+1}^{(j)} \Rightarrow \gamma_{n+1} = \sum_{i=1}^{k_{n+1}} \frac{1}{t_{n+1} - t_{n+1-i}}, \tag{17}$$

which gives a standard formula $\gamma_{n+1} = 1/(t_{n+1} - t_n) = 1/\Delta t_{n+1}$ if the first order (Euler) method is used.

After resolving the linear system (16), the vectors $\boldsymbol{x}_{n+1}^{(\ldots)}$ and $\dot{\boldsymbol{x}}_{n+1}^{(\ldots)}$ are updated

$$\boldsymbol{x}_{n+1}^{(j+1)} = \boldsymbol{x}_{n+1}^{(j)} + \Delta \boldsymbol{x}_{n+1}^{(j)}, \tag{18a}$$

$$\dot{\boldsymbol{x}}_{n+1}^{(j+1)} = \dot{\boldsymbol{x}}_{n+1}^{(j)} + \gamma_{n+1} \Delta \boldsymbol{x}_{n+1}^{(j)}, \tag{18b}$$

which completes the $j+1$ iteration of the $n+1$ time step—however, if an indication of divergence is detected during the iterations, then the logarithmic damping[1] (again, the symbol x marks an element of the vector $\boldsymbol{x}$)

$$\Delta x_{n+1}^{(j)} := \operatorname{sgn}\left(\Delta x_{n+1}^{(j)}\right) \left|x_{n+1}^{(j)}\right| \ln\left(1 + \frac{\left|\Delta x_{n+1}^{(j)}\right|}{\left|x_{n+1}^{(j)}\right|}\right) \tag{19}$$

is used[2] for all the elements of the vector $\Delta \boldsymbol{x}_{n+1}^{(j)}$ before updating to the subsequent values by (18). In the habilitation thesis, another new way protecting the convergence is defined.

3.1.3 Automatic Determination of a New Integration Step and Order

A new length of the integration step Δt_{n+2} and a new order of the polynomial interpolation k_{n+2} are to be chosen after converging the corrector (16) and (18)—the quality of the two procedures is very important for the efficiency of the algorithm.

First, an estimation of the interpolation error in the last integration step must be determined. In general, the *absolute* truncation error for the k_{n+1} order caused by the derivatives approximation (17) may be written as

$$e_{n+1} = \frac{\Delta t_{n+1}}{t_{n+1} - t_{n-k_{n+1}}}\, \delta^{(k_{n+1}+1)} x_{n+1} \tag{20}$$

for any element x_{n+1} of the vector $\boldsymbol{x}_{n+1}$. The relation (20) for the element e_{n+1} of the absolute truncation error vector $\boldsymbol{e}_{n+1}$ must be modified in the following way:

[1] The idea of damping is based on Maclaurin series $\ln(1+x) = x - x^2/2 + x^3/3 - + \cdots \approx x$ for $x \to 0$.

[2] More precisely, $\left|x_{n+1}^{(j)}\right| + \texttt{NULL}$ is used instead of $\left|x_{n+1}^{(j)}\right|$ to avoid possible zero division.

- the absolute errors are replaced by the relative ones (to be comparable with one another and with an algorithm parameter),
- the fraction $\Delta t_{n+1}/(t_{n+1} - t_{n-k_{n+1}})$ is omitted (to give a preference to simpler and more stable lower interpolation orders).

Consequently, the *relative* truncation error of the $n+1$ time step acquires the simple form[3] (again, the proof of the second equality in (21) can be found in [5])

$$\varepsilon_{n+1} = \max_{\forall x_{n+1} \in \boldsymbol{x}_{n+1}} \frac{\left|\delta^{(k_{n+1}+1)} x_{n+1}\right|}{|x_{n+1}|} = \max_{\forall x_{n+1} \in \boldsymbol{x}_{n+1}} \frac{\left|x_{n+1} - x_{n+1}^{(0)}\right|}{|x_{n+1}|}. \tag{21}$$

Therefore, the truncation error may be checked by the difference between the corrector and the predictor and the step may be rejected and halved even after the *first* iteration of the corrector if the truncation error seems too big.

Secondly, the new step and order are determined by means of the error (21). In general, the next possible steps may be estimated using the relative truncation error (21) (Δt_{n+1} is already known when $\Delta t_{n+2}^{(i)}$ should be compared for all possible i and hence is equal $\forall i$)

$$\Delta t_{n+2}^{(i)} = \Delta t_{n+1} \sqrt[i+1]{\frac{\varepsilon}{\varepsilon_{n+1}^{(i)}}}, \ i = 1, \ldots, k_{n+1} + 1, \tag{22}$$

where ε is a prescribed relative truncation tolerance and all the possible truncation relative errors $\varepsilon_{n+1}^{(i)}$ are computed directly by the $\delta^{(i+1)} x_{n+1}$ (that is why the differences (11) are defined up to the $k_n + 2$ order—so that the order of the polynomial interpolation can sequentially increase).

However, the step increase is limited due to the stability conditions, especially for higher orders of interpolation—see the stability comparisons of the basic implicit integration methods in [10]. Thus, the relation (22) must be modified by a semiempirical factor $\sqrt[i+1]{4}$

$$\Delta t_{n+2}^{(i)} = \left\{ \begin{array}{ll} \Delta t_{n+1} \sqrt[i+1]{\dfrac{\varepsilon}{\boxed{4}\,\varepsilon_{n+1}^{(i)}}} & \text{for } \dfrac{\varepsilon}{\boxed{4}\,\varepsilon_{n+1}^{(i)}} < 4, \\ \Delta t_{n+1} \sqrt[i+1]{4} & \text{otherwise,} \end{array} \right\} i = 1, \ldots, k_{n+1} + 1, \tag{23}$$

where the factor $\sqrt[i+1]{4}$ may theoretically be derived under special circumstances only; however, it has been proven by thousands practical analyses, as well. The second semiempirical factor in (23)—the "boxed" 4—serves for an error overestimation (for example, for the Euler method, the new length of the step is underestimated by the factor $0.5 = 1/\sqrt{4}$) to ensure a small number of rejected steps (those with the relative truncation error greater than ε).

In conclusion, the new k_{n+2} order ($k_{n+2} \in \{1, \ldots, k_{n+1} + 1\}$) is chosen, whose step determined by (23) is the longest.

To summarize, the algorithm defined above has the following fundamental merits:

- it is convenient for analyses of the radio frequency and microwave (i.e. fast) devices—let's consider that the very short time steps in (12) are divided by one another (they are *not* multiplied as those in the standard schemes which may cause underflow errors for higher orders of the interpolation polynomials),

[3] Similarly as that in damping, $\left|x_{n+1}^{(j)}\right| + \texttt{NULL}$ is used instead of $\left|x_{n+1}^{(j)}\right|$ to avoid possible zero division.

- the algorithm is more flexible than the Gear's method implemented in PSPICE with respect to quick step and order alterations—the order of the interpolation may change in every step, for instance,
- it is usable in conjunction with the smoothed gate capacitance models for reliable analyses of (practically) arbitrary accuracy—see Table 1 in Section 4,

3.2 A New Formula for the Time Domain Sensitivity Analysis

The algorithm defined above is convenient for the enhancement towards the time domain sensitivity analysis—due to its efficiency, the results are obtained in a reasonable time. A simple methodology of the time domain sensitivity analysis has been defined in [3]. However, it is based on the first order of the interpolation polynomial only. In the habilitation thesis, a new effective formula has been derived using the backward differences (11) of higher order. With respect to the implicit form of (10), a system of parametric algebraic-differential equations of a circuit can be written as

$$\boldsymbol{f}\,[\,\boldsymbol{x}(t,p),\dot{\boldsymbol{x}}(t,p),t,p\,]=\boldsymbol{0}, \tag{24}$$

where p is one of the circuit parameters on which the sensitivities are requested. Differentiating (24) with respect to p, we obtain (using the abbreviations $\boldsymbol{x'}(t,p)\equiv\partial\boldsymbol{x}(t,p)/\partial p$ and $\dot{\boldsymbol{x}}'(t,p)\equiv\partial\dot{\boldsymbol{x}}(t,p)/\partial p$)

$$\frac{\partial\boldsymbol{f}}{\partial\boldsymbol{x}}\,\boldsymbol{x'}(t,p)+\frac{\partial\boldsymbol{f}}{\partial\dot{\boldsymbol{x}}}\,\dot{\boldsymbol{x}}'(t,p)+\frac{\partial\boldsymbol{f}}{\partial p}=\boldsymbol{0}. \tag{25}$$

Using the "algebraization" formula (17), we obtain the effective recurrent scheme (a complete proof is performed in the habilitation thesis)

$$\left[\left(\frac{\partial\boldsymbol{f}}{\partial\boldsymbol{x}}\right)_{n+1}+\gamma_{n+1}\left(\frac{\partial\boldsymbol{f}}{\partial\dot{\boldsymbol{x}}}\right)_{n+1}\right]\boldsymbol{x}'_{n+1}=-\left(\frac{\partial\boldsymbol{f}}{\partial p}\right)_{n+1}+\left(\frac{\partial\boldsymbol{f}}{\partial\dot{\boldsymbol{x}}}\right)_{n+1}\times \boxed{\sum_{l=1}^{k_{n+1}}\alpha_{n+1}^{(l-1)}\delta^{(l-1)}\boldsymbol{x}'_n\sum_{k=l}^{k_{n+1}}\frac{1}{t_{n+1}-t_{n+1-k}}}, \tag{26}$$

which has the same Jacobian as that in (16) (for each p, of course)—therefore, the laborious LU-factorization of that system matrix must be executed *once* for each $t_{n+1}, n=0,\ldots$. The "boxed" part of (26) represents an effective replacement of the classical formulae.

4 Testing the System in Digital and Analog Domains

To demonstrate the models and algorithms implemented in the C.I.A. system, two typical examples from the area of the radio frequency integrated circuits design are solved.

4.1 CMOS Radio Frequency Flip-Flop

The first example has come from the digital circuits domain. A radio frequency CMOS flip-flop in Figure 3 has appeared to be an appropriate convergence test. The flip-flop is an

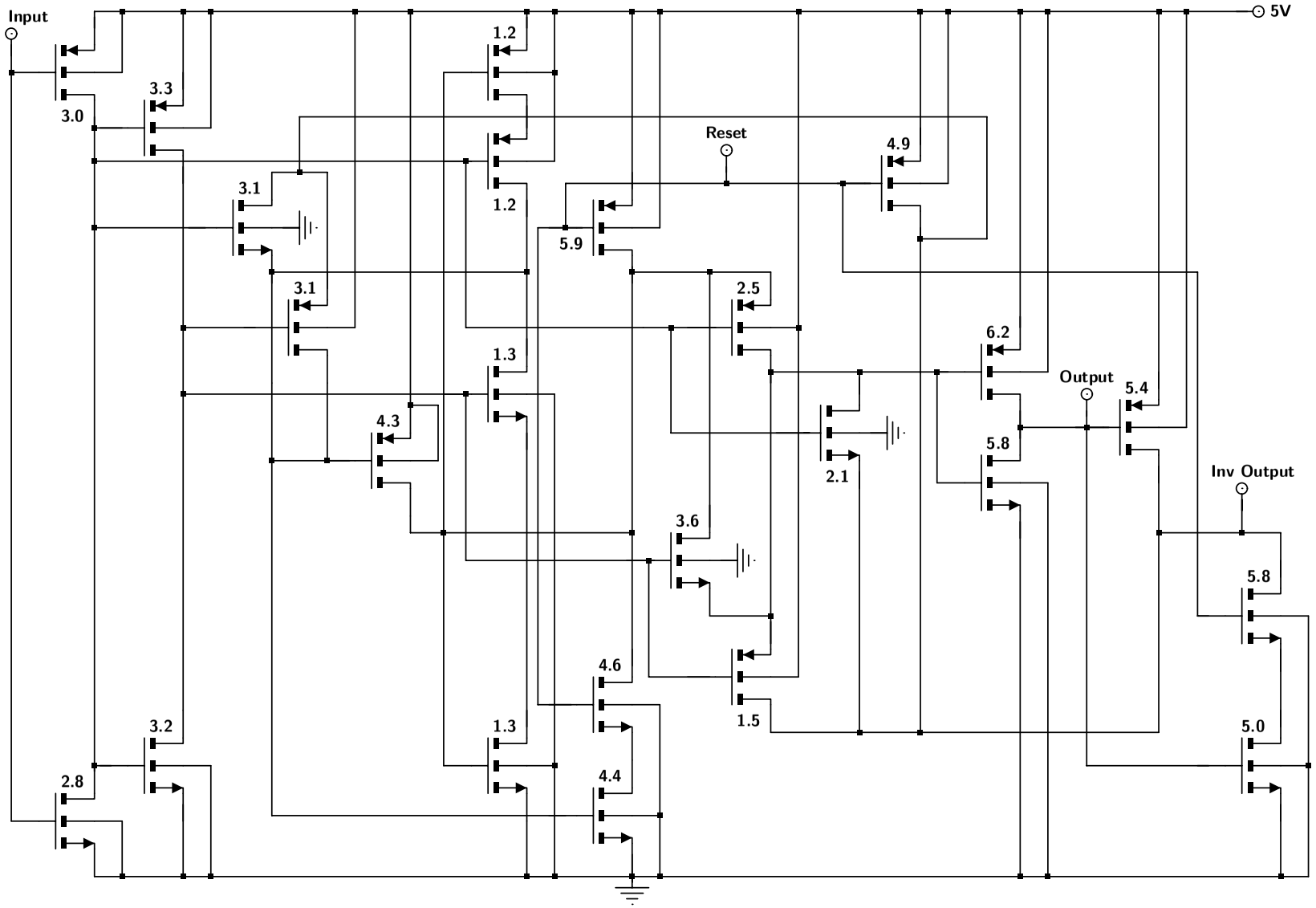

Figure 3: CMOS flip-flop subcircuit used as a test of the model and algorithm—the numbers represent device area factors.

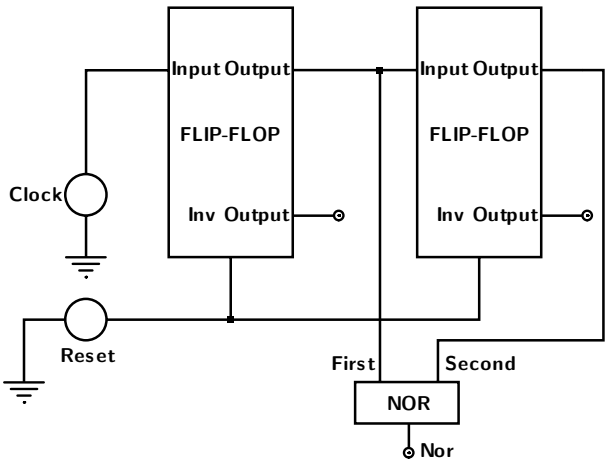

Figure 4: Block diagram of the probed fraction of a large CMOS integrated circuit.

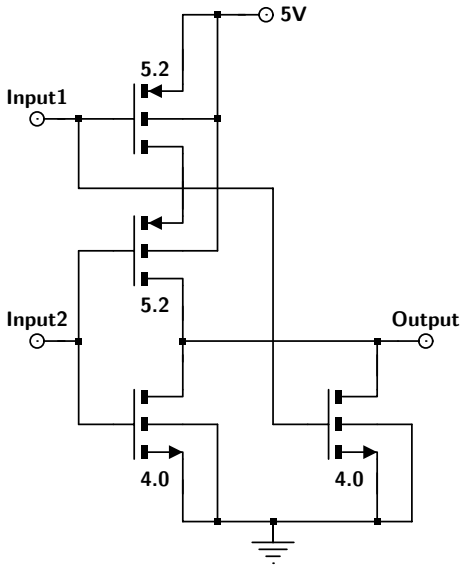

Figure 5: CMOS negative-or subcircuit.

element of a large integrated circuit. However, only a small fraction of the whole circuit is necessary for the test—see Figure 4. The circuit caused serious convergence problems in SPICE analyses, because it contains the transistors which alternate the sign of the drain-source voltage during the transient analysis. Therefore, the analysis has been performed by the algorithm discussed in Section 3. Each of the transistors in the subcircuits FLIP-FLOP and NOR (which processes the outputs of the flip-flops—see Figure 5) is labeled by the SPICE-type `AREA` factor. The threshold voltages and other parameters of the static model are determined for all the transistors from a set of technological parameters.

The gate capacitors are defined by (5a–5e) for the classical model, and by the modifications (8) and (9) for the smoothed one—both are determined by (6) (with the oxide thickness 50 nm) and several parameters of the static model modifying the voltage V_{on} and effective channel length L_{eff}.

The capacitance part of the model is complemented by three linear gate overlap capacitors and, of course, by junction capacitors [8] with the zero-bias bottom capacitances 0.2 pF and the zero-bias perimeter capacitances 0.05 pF.

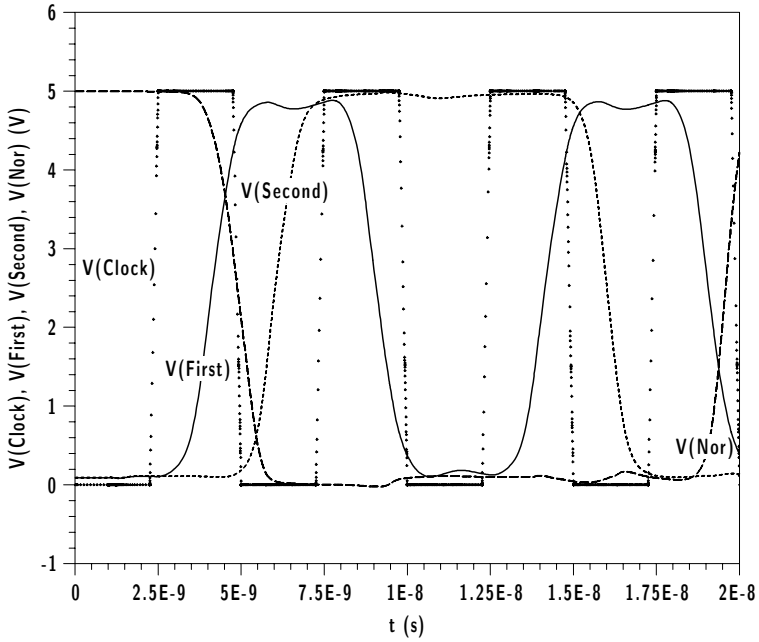

Figure 6: Results of the test—the first flip-flop is switched by the clock signal, the second is switched by the first one. The dotted clock signal shows the automatic step generation.

The results of the analysis are shown in Figure 6. Table 1 summarizes the fundamental differences between the analyses of the test circuit with the classical and updated models of Section 2 by the algorithm of Section 3. As expected and also received by SPICE analyses, the results using classical models show several non-convergences: here, for 200 MHz clock signal with 250 ps rise and fall times, 5 and 10 non-convergences occurred for $\varepsilon = 5 \times 10^{-3}$ and $\varepsilon = 2 \times 10^{-3}$, respectively—even for the maximum number of iterations allowed in one integration step `MAXIT` = 200. Let's emphasize that *huge* numbers of non-convergences have been received for the classical Meyer's model if $\varepsilon \leqq 10^{-3}$, and therefore such analyses are practically impossible.

Task specification by		Total number of			
capacitan. model	ε	non-conver.	solv. lin. syst.	LU factoriz.	log. damp.
Meyer classical†	10^{-2}	0	2193	1650	0
	5×10^{-3}	**5**	3575	2903	987
	2×10^{-3}	**10**	5550	4525	1978
Meyer smoothed	10^{-2}	0	2153	1612	0
	5×10^{-3}	0	2484	1853	0
	2×10^{-3}	0	3217	2349	0
	10^{-3}	0	3671	2678	0
	10^{-4}	0	7117	5150	0
	10^{-5}	0	12634	9235	0
	10^{-6}	0	21020	15446	0

†Analyses with the classical model cause a lot of non-convergences if the truncation error $\varepsilon \leqq 10^{-3}$.

Table 1: Comparison of the results obtained using the classical and smoothed models.

Moreover, the problems with convergence cause a number of logarithmic dampings (19) to be used in the case of classical model and, which is the worst, the number of LU factorizations of the Jacobian in (16) to be executed is considerably higher.

As an illustration of the algorithm flexibility, let's compare the results for the smoothed model if the relative truncation tolerance ε varies from 10^{-2} to 10^{-6} (the first and last rows for the smoothed model)—while the error is 10,000 times lesser, the number of necessary LU factorizations is only 10 times greater!

4.2 CMOS Radio Frequency Four-Quadrant Multiplier

Let's consider a four-quadrant low-voltage low-power CMOS RF multiplier [11] in Figure 7 which has been checked using the sensitivity analysis defined in Subsection 3.2. All the parameters of the MOSFET models have been kindly granted by prof. Salama [11].

The output voltage of the multiplier is dependent on the controlling one—see the source connected to the gates of m6 and m7 transistors. A comparison of the output signals for the two controlling voltages is shown in Fig. 8. For the controlling voltages 1 and 1.5 V, the magnitudes of the output signal are about 20 and 50 mV, respectively.

The output voltage of the multiplier is also very dependent on the zero-bias threshold voltages (V_{T0}) of the transistors. The sensitivities of the output voltage on the zero-bias threshold voltages, i.e., the functions $\partial V_{\mathrm{Output}}/\partial V_{T0,\mathrm{MN1}}\,(t)$, $\partial V_{\mathrm{Output}}/\partial V_{T0,\mathrm{MN2}}\,(t)$, and $\partial V_{\mathrm{Output}}/\partial V_{T0,\mathrm{MP}}\,(t)$ are shown in Figure 9. As observed, the sensitivity on the threshold voltage $V_{T0,\mathrm{MP}}$ is the most significant.

The results in Figure 9 can be simply checked. The zero-bias threshold voltages of the MN and MP transistors were 0.47 and 0.44 V, respectively. Let's emphasize that the C.I.A. model uses another definition for the zero-bias threshold voltages—the original values of the standard PSPICE type model were 0.62 and -0.58 V [11] (in the C.I.A. model, the threshold voltage is *positive* for both N and P channel enhancement mode transistors). We can execute another analysis with somewhat changed $V_{T0,\mathrm{MP}}$ parameter and estimate the sensitivity numerically. For example, let's use a modified value $V'_{T0,\mathrm{MP}} = 0.4$ V. At 17 ns (where the sensitivity of V_{Output} on $V_{T0,\mathrm{MP}}$ has the local maximum 0.0379411—see Figure 9), the values of the output voltages V_{Output} and V'_{Output} (computed using the values $V_{T0,\mathrm{MP}} = 0.44$ V and $V'_{T0,\mathrm{MP}} = 0.4$ V) were 0.0139211 V and 0.0118593 V, respectively. Now let's compare the results: the predicted value obtained using the sensitivity is $V''_{\mathrm{Output}} = 0.0139211 - 0.04 \times 0.0379411 = 0.0124035$ V, the actual output obtained using the value $V'_{T0,\mathrm{MP}}$ is $V'_{\mathrm{Output}} = 0.0118593$ V, so the error of the prediction is about 4.59 %. At 20 ns, the values of V_{Output}, $\partial V_{\mathrm{Output}}/\partial V_{T0,\mathrm{MP}}$, and $V'_{T0,\mathrm{MP}}$ were 0.00152467 V, 0.00303789, and 0.00138769 V, respectively. Comparing again, the predicted value obtained using the sensitivity is $V''_{\mathrm{Output}} = 0.00152467 - 0.04 \times 0.00303789 = 0.00140315$ V, the actual output obtained using the modified value $V'_{T0,\mathrm{MP}}$ is $V'_{\mathrm{Output}} = 0.00138769$ V, so the error of the prediction is about 1.11 % now.

If we want to execute the sensitivities on the zero-bias threshold voltages only, the above experiments using modified values V'_{T0} are possible. However, the semiempirical, BSIM, and EKV models have a lot of parameters and therefore it is impossible to check the circuit using differences of the model parameters if we want to check *all* the sensitivities. Emphasize that the symmetrical circuit in Figure 7 has *zero* static sensitivities (on principle). Hence, the PSPICE sensitivity analysis does not offer any usable results here.

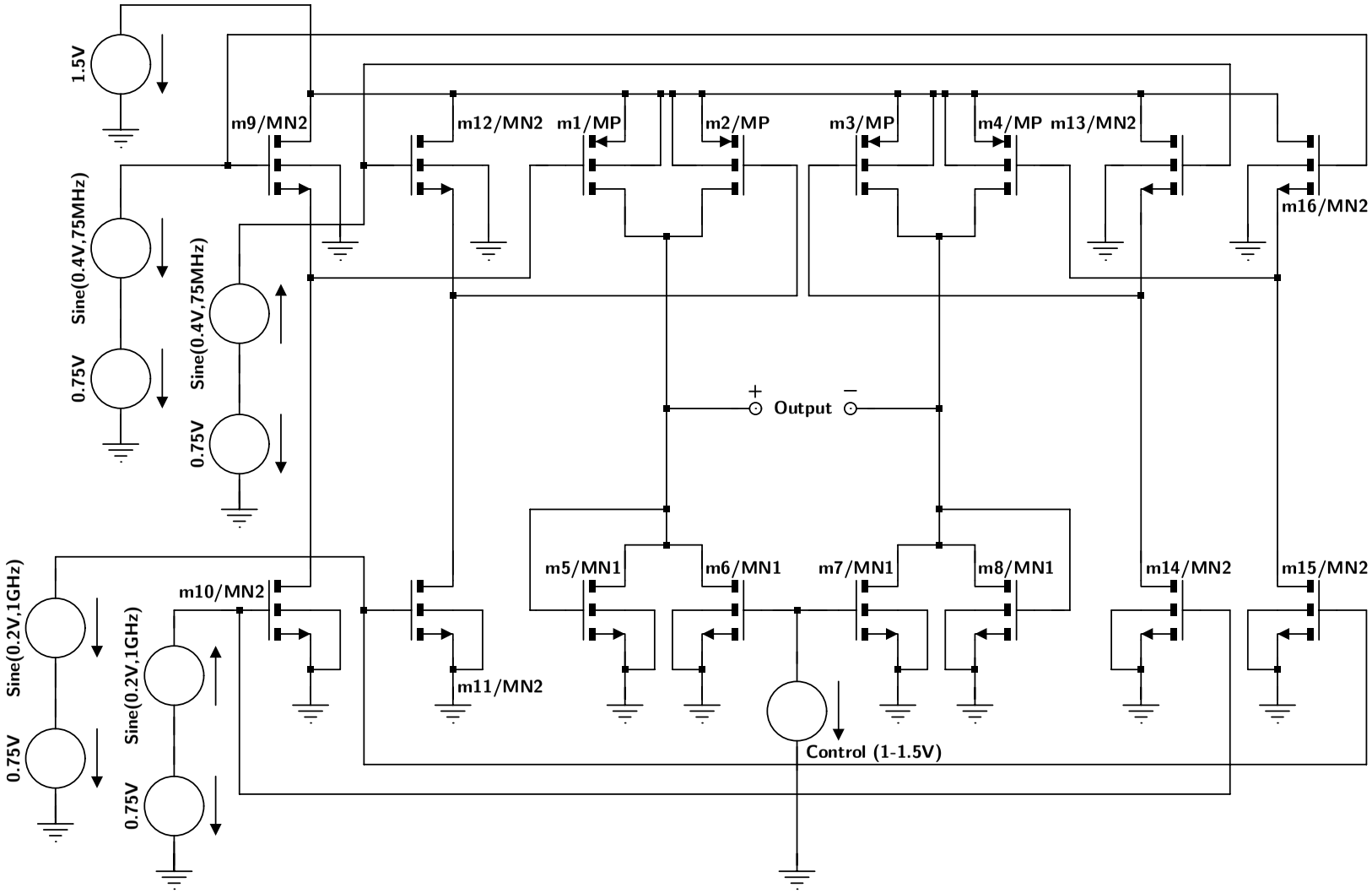

Figure 7: Low-voltage low-power CMOS RF four-quadrant multiplier with symmetrical LF (input signal) and HF (local oscillator) sources.

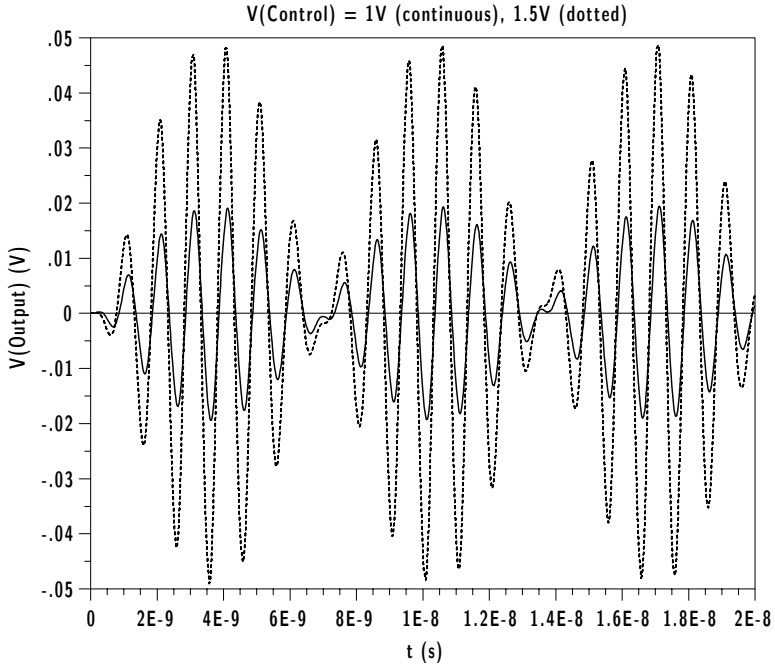

Figure 8: Dependence of the multiplier output voltage on the controlling voltage.

5 Conclusions

The accuracy and reliability of the analyses are influenced by the model qualities. In this area, the ways for improving the classical models of GaAsFET and MOSFET have been presented. The effective, flexible and stable algorithm for solving the nonlinear systems of algebraic-differential equations has been characterized with the new embedded recurrent formula for the time domain sensitivity analysis. The model and algorithm properties are demonstrated by solving two examples from the radio frequency integrated circuit design.

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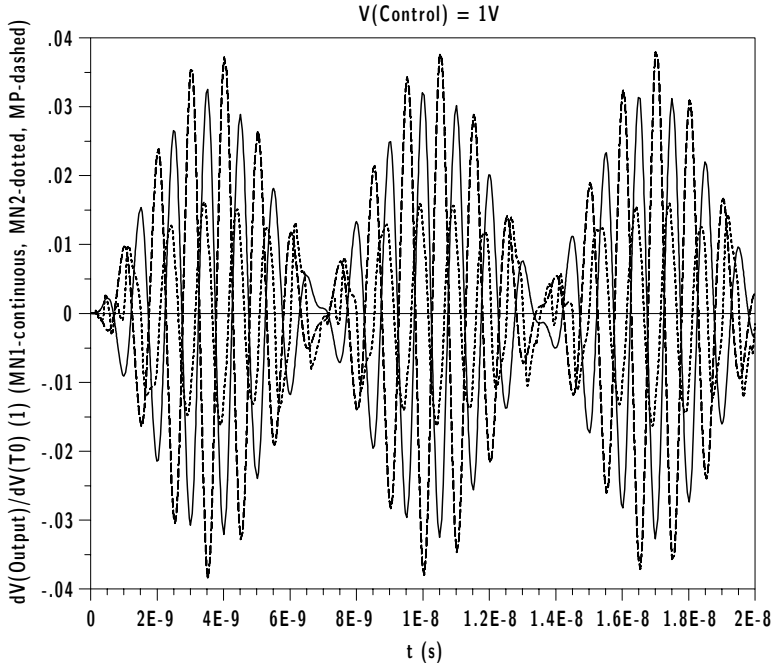

Figure 9: Sensitivities of the multiplier output voltage on the zero-bias threshold voltages of the MN1, MN2, and MP transistors.

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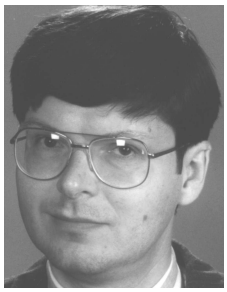
Ing. Josef Dobeš, CSc.



Date and place of birth: April 26, 1958 in Chlumec nad Cidlinou

Affiliation: Czech Technical University in Prague, Faculty of Electrical Engineering, Department of Radio Engineering
Postal address: Technická 2, 16627 Praha 6 – Dejvice, Czech Republic
E-mail address: dobes@feld.cvut.cz (or alias j.dobes@ieee.org)

Education:
1982 – M.S. (Ing.) at the Department of Microelectronics, Czech Technical University
1986 – Ph.D. (CSc.) – „ –

Brief chronology of employment:

1982–1986	Postgraduate student	Department of Microelectronics, CTU FEE
1986–1992	Research fellow	TESLA Research Institute (TESLA VÚST)
since 1992	Assistant professor	Department of Radio Engineering, CTU FEE

Stages and study leaves:

1989	Process simulators	Zentrum Mikroelektronik, Frankfurt (Oder)
1992	Device simulators	Institute of Microelectronics, Sophia
1992	Circuit simulators	MATRA Systems UK Ltd., Munich

Current service activities:
Deputy head of the Department of Radio Engineering
Member of the Academic Senate of the Faculty of Electrical Engineering

Journal editorial boards: Radioengineering (2003–2004), Electronic Horizon (in 2004)

Membership in societies: (FRVŠ=Foundation of the Universities Development)
IEEE: Czechoslovakia Joint CAS/COM/SP Chapter – since 2000 (chairman since 2004)
Czechoslovakia Joint ED/MTT/AP Chapter – since 2000
National Committee of the Czechoslovakia Section – since 2004
FRVŠ: National Committee of the Foundation – 2000–2002

Teaching experience:
Lectures: since 1994 – Computer-Aided Design of Radio Frequency Circuits
1997–1999 – Software Equipment for Radio Engineering
since 2000 – Basics of Radio Engineering
Supervising of graduate students: 10 successfully graduated (6 M.S., 4 B.S.) students
Supervising of Ph.D. students: 1 successful Ph.D. student, currently 5 Ph.D. students

Publication activity: Over 80 journal and conference papers

Industrial application: Author of the C.I.A. (Circuit Interactive Analyzer) program

Main grant support: (GAČR=Czech Science Foundation, EC=European Commission)

GAČR	2001–2003	"Symbolic, Semisymbolic, and Numerical Methods of Analysis, Design, and Optimization of Electrical Circuits"
EC	since 2004	"TARGET – Top Amplifier Research Groups in a European Team"

Research areas:
Modeling of circuit elements, especially RF and microwave transistors and transmission lines, creating or improving algorithms for the circuit analysis and optimization, such as time- and frequency-domain sensitivity, poles-zeros or steady-state analyses, creating a comprehensive CAD tool for the analysis and optimization of RF and microwave circuits.